UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,762	07/06/2004	Heinz Van Der Broeck	DE 020013	7172

7590 09/19/2006

Philips Electronics North America Corporation
Corporate Patent Counsel
PO Box 3001
Briarcliff Manor, NY 10510

EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,762	VAN DER BROECK ET AL.	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 29** is objected to because of the following informalities: Grammatical Errors.

The second line of claim 29 should read as follows:

Supplying AC voltage to the plasma display panel, which the circuit arrangement

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claim 14** recites the limitation "the AC voltage supply" in line 1. There is insufficient antecedent basis for this limitation in the claim.

3. **Claim 8** recites the limitation "the auxiliary capacitor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1, 2, 5-9, and 14-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai (Patent No.: 6,011,355) in view of Yao et al. (Patent No.: 5,844,373).

With respect to **Claim 1**, Nagai discloses a circuit arrangement for an AC voltage supply of a plasma display panel *(column 8, lines 6-8; note that the seventh embodiment builds upon previous embodiments)*, the arrangement comprising: a transistor bridge having a pair of voltage input nodes and a pair of voltage output nodes *(See figure 6, where the transistor bridge is comprised of elements 26, 28, 38, and 39)*, an input voltage *(Vcc)* coupled to the pair of voltage input nodes of the transistor bridge, a capacitor of a plasma cell *(See figure 19, Cp)* coupled to the pair of voltage output nodes of the transistor bridge, and a charging current circuit *(See figure 6, elements 22a and 23a)*. Nagai does not mention the charging current circuit to receive an auxiliary charging voltage from a DC voltage converter so as to provide charging current to the capacitor.

Yao teaches a charging current circuit *(See figure 6)* receiving an auxiliary charging voltage *(voltage flowing across C3; Vw ~ auxiliary charging voltage; Note that a parallel connection is at the point common to elements T1, D1, and C4)*, from a DC voltage converter *(3b ~ DC voltage converter; Note, that Va is a direct current voltage; column 4, line 66-67 and column 5 lines 24-26)* so as to provide a charging current. Yao teaches the DC voltage converter provides the auxiliary charging voltage from an input voltage *(See figure 6, Vs)*. Yao modifies the circuit arrangement of Nagai by connecting the voltages Vw and Va respectfully to the source electrode of element 22a and 22b of Nagai, resulting in a circuit arrangement of a

charging current circuit that receives the auxiliary charging voltage and provides charging current to the capacitor. The capacitor 21 of Nagai is removed.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have the charging current circuit to receive an auxiliary charging voltage from a DC voltage converter so as to provide charging current, as taught by Yao to the circuit arrangement of Nagai for the purpose of generating a steady and smooth direct current voltage *(Yao: column 5, lines 25-26).*

With respect to **Claim 29**, Claim 29 differs from claim 1 only in that Claim 29 is a plasma display panel comprising a circuit arrangement of claim 1 and Claim 1 is a circuit arrangement for a plasma display panel. Claim 29 and Claim 1 are essentially equivalent claims differing in that claim 1 recites the limitation "... the charging current circuit ..." and claim 29 recites the limitation "... the charging circuit ...". Claim 29 is broader than claim 1, thus claim 29 is analyzed as previously discussed with respect to claim 1.

With respect to **Claim 14**, Nagai discloses a circuit arrangement for an AC voltage supply of a plasma display panel *(column 8, lines 6-8; note that the seventh embodiment builds upon previous embodiments)*, the arrangement comprising: a transistor bridge *(See figure 6, where the transistor bridge is comprised of elements 26, 28, 38, and 39)* having a pair of voltage input nodes and a pair of voltage output nodes, an input voltage *(Vcc)* coupled to the pair of voltage input nodes of the transistor bridge, a capacitor of the plasma cell *(See figure 19, Cp)* coupled to the pair of voltage output nodes of the transistor bridge, and a discharging circuit *(See*

figure 6, elements 22b and 23b). Nagai does not teach the discharging circuit to receive an auxiliary discharging voltage from a DC voltage converter so as to provide discharging current to the capacitor.

Yao teaches an auxiliary discharging voltage *(See figure 6, voltage across C4)*, where a DC voltage converter *(3b ~ DC voltage converter; Note, that Va is a direct current voltage; column 4, line 66-67 and column 5 lines 24-26)* is connected in parallel to the auxiliary discharging voltage *(voltage across C4 ~ discharging voltage; Note that the parallel connection is at the point common to elements T1, D1, and C4)* for providing a discharging current. Yao teaches the DC voltage converter provides the auxiliary discharging voltage from an input voltage *(See figure 6, Vs)*. Yao modifies the circuit arrangement of Nagai by connecting the voltages Vw and Va respectfully to the source electrode of element 22a and 22b of Nagai, resulting in a circuit arrangement having a discharging circuit to receive an auxiliary discharging voltage from a DC voltage converter so as to provide discharging current to the capacitor of a plasma cell. The capacitor 21 of Nagai is removed.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have the discharging circuit to receive an auxiliary discharging voltage from a DC voltage converter so as to provide discharging current to the capacitor, as taught by Yao to the circuit arrangement of Nagai for the purpose of generating a steady and smooth direct current voltage *(Yao: column 5, lines 25-26)*. The circuit arrangement of Nagai is modified by connecting in parallel the charging current circuit of Yao by connecting the voltage Vw and Va respectfully to the source electrode of element 22a and 22b of Nagai.

With respect to **Claim 2**, the circuit arrangement of claim 1, Nagai does not teach the the DC voltage converter is a boost converter.

Yao teaches the DC voltage converter is a boost converter *(See figure 6, element 2b is a voltage booster; column 5, lines 27-34).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a DC voltage converter that is a boost converter, as taught by Yao, to the circuit arrangement of Nagai for the purpose of having a stabilized voltage that is amplified to a high voltage *(Yao: column 5, lines 39-41, and column 4, lines 66-67).*

With respect to **Claim 5**, the circuit arrangement of claim 1, Nagai does not teach the auxiliary charging voltage is greater than half the input voltage.

Yao teaches the auxiliary charging voltage *(See figure 6, Vw = 150 V ~ auxiliary charging voltage)* is greater than half the input voltage *(Vs = 180 V ~ input voltage).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have an auxiliary charging voltage greater than half the input voltage, as taught by Yao, to the charging current circuit of Nagai so as to generate an entire-surface discharge voltage that results from adding the boosted stabilized voltage Vw to the stabilized voltage Va such that a switching regulator is unnecessary *(Yao: column 3, lines 23-29, column 4, lines 66-67, and column 5, lines 39-41)* and to provide a small-sized and economical power unit *(Yao: column 2, lines 45-47).*

With respect to **Claim 6**, the circuit arrangement of claim 1, Nagai teaches the charging current circuit includes a series combination of a charging transistor *(See figure 6, 22a)*, a charging diode *(23a)* and a charging inductor *(LX)*.

With respect to **Claim 7**, the circuit arrangement of claim 1, Nagai does not teach the auxiliary charging voltage is applied to an auxiliary capacitor.

Yao teaches the auxiliary charging voltage *(See figure 6, Vw)* is applied to an auxiliary capacitor *(C3)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary charging voltage applied to an auxiliary capacitor, as taught by Yao, to the charging current circuit of Nagai for the purpose of obtaining the voltage Vw through the charging of capacitors C1, C2, and C3 *(Yao: column 5, lines 28-35 and lines 64-67)*.

With respect to **Claim 8**, the circuit arrangement of Nagai as modified by Yao in claim 1, teaches a capacitance *(Yao: See figure 6, Note that the auxiliary capacitor is a combination of C1, C2, and C3)* of an auxiliary capacitor is much larger than a capacitance of the capacitor *(Yao: See figure 4, 1a ~ plasma panel; the capacitor of the plasma cell is representative a one pixel)* of the plasma cell. The voltage across the capacitors C1, C2, and C3 is greater than the input voltage and the combination of the capacitors and must be larger than the capacitance of a plasma cell since the voltage Vd *(Yao: Vd ~ Vw +Va; column 3, lines 23-29)* is for generating the entire-surface discharge voltage for the display.

With respect to **Claim 9**, the circuit arrangement of claim 1, Nagai does not teach the DC voltage converter provides an auxiliary discharging voltage and the auxiliary charging voltage is generated from the auxiliary discharging voltage.

Yao teaches the DC voltage converter *(3b ~ DC voltage converter; Note, that Va is a direct current voltage; column 4, line 66-67 and column 5 lines 24-26)* provides an auxiliary discharging voltage *(Va; See figure 6, voltage across C4)* from an input voltage *(See figure 6, Vs)*. Yao teaches an auxiliary charging voltage *(See figure 6, Vw)* is generated from an auxiliary discharging voltage.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a DC voltage converter to provide an auxiliary discharging voltage such that the auxiliary charging voltage is generated from an auxiliary discharging voltage, as taught by Yao to the circuit arrangement of Nagai so as to generate a constant auxiliary charging voltage since the auxiliary discharging voltage is stabilized and used to generate the auxiliary charging voltage *(Yao: column 4 lines 66-67 and column 5, lines 31-35)*.

With respect to **Claim 28**, the circuit arrangement of claim 1, Nagai teaches a common input voltage *(See figure 6, Vcc)* used for a plurality of independent bridge circuits *(26, 28, 38 and 39 form a bridge circuit)*. Nagai does not teach the DC voltage converter provides an auxiliary discharging voltage from the input voltage, and the auxiliary charging and discharging voltages are used for a plurality of independent bridge circuits that are coupled to the input voltage.

Yao teaches auxiliary voltages *(See figure 6, Va and Vw ~ auxiliary voltages)* and the associated DC voltage converters *(3b)*.

The circuit arrangement *(figure 6)* of Nagai is modified by Yao to meet the limitation of the DC voltage converter providing an auxiliary discharging voltage from the input voltage, such that the auxiliary charging and discharging voltages are used for a plurality of independent bridge circuits that are coupled to the input voltage by connecting the voltages Vw and Va of Yao to the source electrodes 22a and 22b respectively of Nagai.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the auxiliary voltages of Yao to the circuit arrangement of Nagai so as to output a stabilized voltage for charging *(Yao: column 4, lines 66-67)*.

With respect to **Claim 15**, the circuit arrangement of claim 14, Nagai does not teach a DC voltage converter is a buck converter.

Yao teaches a DC voltage converter is a buck converter *(See figure 6, the buck converter is comprised of elements To, D3 and L; column 5, lines 19-27)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a DC voltage converter that is a buck converter, as taught by Yao to the circuit arrangement of Nagai for the purpose of outputting a stabilized voltage Va *(Yao: column 4, lines 66-67)*.

With respect to **Claim 16**, the circuit arrangement of claim 15, Nagai does not teach the buck converter comprising a supply transistor, a supply diode and a supply inductor.

Yao teaches a buck converter comprising a supply transistor *(See figure 6, To)*, a supply diode *(D3)* and a supply inductor *(L)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a buck converter comprising a supply transistor, a supply diode, and an supply inductor, as taught by Yao to the circuit arrangement of Nagai for the purpose of outputting a stabilized voltage Va *(Yao: column 4, lines 66-67)*.

With respect to **Claim 17**, the circuit arrangement of claim 15, Nagai does not teach a buck converter is connected to a positive side of the input voltage, a negative side of the input voltage, and to an auxiliary discharge capacitor that stores the discharge voltage.

Yao teaches a buck converter is connected to a positive side of the input voltage, a negative side of the input voltage, and to an auxiliary discharge capacitor that stores the discharge voltage *(See figure 6, where the buck converter is element 3b, comprising elements To, D3, and L; the input voltage Vs inherently has a positive side and a negative side, and therefore is connected to the capacitor C4)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a buck converter that is connected to a positive side of the input voltage, a negative side of the input voltage, and to an auxiliary discharge capacitor that stores the discharge voltage, as taught by Yao to the circuit arrangement of Nagai so as to produce a steady and smooth direct current voltage *(Yao: column 5, lines 25-27)*.

With respect to **Claims 18 and 27**, the circuit arrangement of claims 14 and 21, Nagai does not teach an auxiliary discharging voltage is less than half the input voltage.

Yao teaches an auxiliary discharging voltage *(See figure 6, Va = 50 V)* has a value that is less than half the input voltage *(Vs = 180 V)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary discharging voltage having a value that is less than half the input voltage, as taught by Yao to the circuit arrangement of Nagai so as to provide a small-sized and economical power unit *(Yao: column 2, lines 45-47)* since the discharging voltage is used for generating pulses to the scanning electrodes *(Yao: column 4, lines 11-15)* and for generation of a boosted voltage *(Yao: boosted voltage ~ Vw, column 5, lines 32-35)* that is later used for generating an entire-surface discharge for the display *(Yao: Vd ~ entire-surface discharge voltage; column 3, lines 25-29)*.

With respect to **Claim 19**, the circuit arrangement of claim 14, Nagai teaches the discharging circuit includes a series combination of a discharging transistor *(See figure 6, 22b)*, a discharging diode *(23b)* and a discharging inductor *(LX)*.

With respect to **Claim 20**, the circuit arrangement of claim 14, Nagai does not teach the auxiliary discharging voltage is applied to an auxiliary discharging capacitor.

Yao teaches an auxiliary discharging voltage (*See figure 6, Va)* is applied to an auxiliary discharging capacitor *(C4)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an auxiliary discharging voltage applied to an auxiliary discharging capacitor, as taught by Yao to the circuit arrangement of Nagai so as to output a steady and smooth direct-current voltage through an auxiliary discharging capacitor *(Yao: column 5, lines 24-26)*.

With respect to **Claim 21**, the circuit arrangement of claim 20, Nagai does not mention a capacitance of the auxiliary discharging capacitor is significantly greater than a capacitance of the plasma cell.

Yao teaches the capacitance *(See figure 6, Note that the auxiliary discharging capacitor is equivalent to C4)* of the auxiliary discharging capacitor is significantly greater than a capacitance of the plasma cell *(See figure 4, 1a ~ plasma panel; the capacitor of the plasma cell is representative a one pixel)*. The auxiliary discharging capacitor stores the voltage for supplying pulses to the scanning electrodes *(column 4, lines 13-15)*; therefore the auxiliary capacitor must by far exceed that of a plasma cell since the stored voltage is for the entire display.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a capacitance value of the auxiliary discharging capacitor to by far exceed the capacitance of a plasma cell, as taught by Yao to the circuit arrangement of Nagai for the purpose of generating pulses to all the scanning electrodes *(Yao: column 4, lines 13-15)* and providing a small-sized and economical power unit *(Yao: column 2, lines 45-47)*.

With respect to **Claim 22**, the circuit arrangement of Nagai as modified by Yao in claim 14, teaches the auxiliary discharging voltage *(Yao: See figure 6, Va)* is generated from a discharge of the capacitor of the plasma cell and stabilized by the DC voltage converter *(column 4, lines 66-67; column 5, lines 24-27)*.

With respect to **Claim 23**, the circuit arrangement of claim 22, Nagai does not teach a DC converter compensates for losses caused by commutation and takes power from the input voltage.

Yao teaches a DC converter. The DC converter of Yao is constructed in such a way that the PWM-control IC *(Yao: figure 6, 30)* regulates the power supply voltage Va despite various variations in load *(column 5, lines 6-15)*. Referring back to the modification of the circuit arrangement of Nagai by Yao as discussed in claim 14, if loss is caused by commutation then the PWM-control IC will lengthen the "ON" period of the transistor *(To)* to compensate for the losses. Thus, Yao teaches a DC voltage converter when incorporated into the circuit arrangement of Nagai compensates for the losses caused by commutation and takes power from the input voltage.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use the DC converter of Yao to the circuit arrangement of Nagai so as to output a steady and smooth direct-current voltage *(Yao: column 5, lines 24-27)*.

With respect to **Claim 24**, the circuit arrangement of claim 16, Nagai does not teach the supply transistor shares a first common connection point with a positive side of the input voltage

and shares a common connection point with the supply inductor and an anode of the supply diode.

Yao teaches a supply transistor *(figure 6, To)* shares a first common connection point with the input voltage *(Vs)* and shares a common connection point with the supply inductor *(L)* and the anode of the supply diode *(D3)*. Please note that the source and drain are identical electrodes, thus the direction of current should not matter and the source and drain of the transistor of Yao are interchangeable.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a transistor have one electrode other than the gate electrode connected to the input voltage and the other electrode other than the gate electrode connected to the coil such that the anode of the diode is connected at the same point as the coil and electrode of a transistor, as taught by Yao to the circuit arrangement of Nagai, so as to generate a steady and smooth direct-current voltage *(column 5, lines 24-27)*.

With respect to **Claim 25**, due to the broadness of the claim there exists two alternative connections that reads on the claim limitations. The first alternative is taught solely by Nagai and the teaching is as follows, Nagai teaches a supply inductor *(See figure 6, LX)* is connected to a discharging transistor *(22b)* of the discharging circuit.

The second alternative is by way of the modified circuit as explained previously in the analyzing of claim 14 where the supply inductor *(Yao: Figure 6, L)* is connected to the discharging transistor *(Nagai: figure 6, 22b)* of the discharging circuit at the voltage Va *(Note that the elements 21 and 22b of Nagai are connected in parallel to the voltage booster 2b of*

Yao). It would haven been obvious for a person of ordinary skill in the art at the time the invention was made to modify the circuit of Nagai by connecting a supply inductor to a discharging transistor of the discharging circuit, as taught by Yao so as to output a steady and smooth direct-current voltage *(Yao: column 5, lines 19-27)*.

With respect to **Claim 26**, the circuit arrangement of Nagai as modified by Yao in claim 25, teaches the supply inductor *(Yao: figure 6, element L)* is connected to at least a charging transistor *(Nagai: figure 6, element 22a)* of a charging circuit *(Nagai: figure 6, elements 22a, 23a)*. The connection of the inductor *(Yao: figure 6, element L)* is through the electrode common to the anode and cathode of a diode *(Yao: figure 6, element D1)* and to the charging transistor *(Nagai: figure 6, 22a)*.

2. **Claims 3-4 and 10-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai and Yao as applied to claim 1 above, and further in view of Breunig et al. (Pub. No.: 2001/0023488).

With respect to **Claim 3**, the circuit arrangement of claim 2, Neither Nagai nor Yao teach the boost converter comprising a supply transistor, a supply diode, and a supply inductor.

Breunig teaches a boost converter *(See figure 2b)* comprising a supply transistor *(62)*, a supply diode *(66)*, and a supply inductor *(64)*. The circuit arrangement of Nagai, modified by Yao is further modified by Breunig by replacing the voltage booster *(figure 6, 2b)* of Yao with the boost subsystem *(figure 2b, 6)* of Breunig. The input to the supply inductor *(Breunig: 64)* is

connected to the source electrode of the transistor 22b of Nagai, the common connection point of the supply inductor, supply transistor and supply diode *(Breunig: 64, 62, and 66)* is connected to the direct current voltage *(Yao: Va)* and the connection point of the supply diode and capacitor *(Breung: 66 and 68)* is connected to the source electrode of the transistor 22a of Nagai.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a boost converter comprising a transistor, diode, and an inductor, as taught by Breunig to the circuit arrangement of Nagai as modified by Yao so as to supply voltage in the event that the input voltage supply produces an insufficient supply level *(Breunig: page 1, [0017], lines 7-11)*.

With respect to **Claim 4**, the circuit arrangement of Nagai as modified by Yao and Breunig in claim 3 teaches the DC voltage converter *(Breunig: See figure 2b)* provides the auxiliary charging voltage *(Breunig: cathode of the diode 66)* to a charging capacitor *(Breunig: element 68)*, and an auxiliary discharging voltage *(Yao: figure 6, Va)* to a discharge capacitor *(Yao: element C4)*, and the inductor *(Breunig: element 64)* and diode *(Breunig: element 66)* are arranged in series between the charging capacitor *(Breunig: element 68)* and discharging capacitor *(Yao: figure 6, C4)*. Note that the modified circuit of Nagai by both Yao and Breunig has a common connection among all the circuits at the source electrode of 22b of Nagai such that auxiliary discharging voltage Va of Yao and the input to the supply inductor of Breunig allow for the supply inductor and supply diode to be connected in series between the charging and discharging capacitors.

With respect to **Claim 10**, the circuit arrangement of claim 3, neither Nagai nor Yao teach the supply transistor shares a first connection point with an auxiliary charging capacitance that stores the auxiliary voltage and a ground terminal of the input voltage and a second connection point shared with the supply inductor and an anode of the supply diode.

Breunig teaches the supply transistor *(figure 2b, 62)* shares a first connection point *(GND)* with an auxiliary charging capacitance *(68)* that stores the auxiliary voltage and a ground terminal of the input voltage *(the input voltage is inherently known to have a ground terminal)* and a second connection point *(the point common to elements 62, 64, and 66)* shared with the supply inductor and an anode of the supply diode.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have the supply transistor share a first connection point with an auxiliary charging capacitance that stores the auxiliary voltage and a ground terminal of the input voltage and a second connection point shared with the supply inductor and an anode of the supply diode, as taught by Breunig to the circuit arrangement of Nagai as modified by Yao so as to supply voltage in the event that the input voltage supply produces an insufficient supply level *(Breunig: page 1, [0017], lines 7-11)*.

With respect to **Claim 11**, the circuit arrangement of Nagai as modified by Yao and Breunig in claim 10 teaches a cathode of the supply diode *(Breunig: figure 2B, element 66)* has a connection point shared with a charging transistor *(Nagai: figure 6, elements 22a)* of the charging current circuit *(Nagai: figure 6, elements 22a and 23a)* and the auxiliary charging capacitor *(Breunig: figure 2B, element 68)*.

With respect to **Claim 12**, the circuit arrangement Nagai as modified by Yao and Breunig in claim 10 teaches the supply inductor *(Breunig: figure 2B, element 64)* is connected at least to a discharging transistor *(Nagai: figure 6, elements 22b)* of a discharging current circuit *(Nagai: figure 6, elements 22b and 23b).*

With respect to **Claim 13**, there are no differences in the limitations between claim 13 and claim 5. The only difference between claim 13 and claim 5 are claims from which they depend, thus claim 13 is analyzed as previously discussed with respect to claim 5.

Response to Arguments

3. Applicant's arguments filed 7/6/2006 have been fully considered but they are not persuasive.

Applicant argues that neither Nagai nor Yao teaches or suggest an auxiliary voltage supply to provide the charging current to plasma cells. The examiner is not required to provide the same motivation for combining references as the applicant for the end result and the combination of references by the examiner is to have the same result, namely an auxiliary voltage supply to provide the charging current to plasma cells.

Applicant alleges that the combination of Nagai and Yao is inoperable because the circuit of Nagai operates by maintaining the voltage at the source electrodes of elements 22a and 22b essentially constant at half the input voltage and that Yao teaches Vw is generated to be three times the value of Va. The examiner cannot see anywhere in Nagai's specification such an

allegation of maintaining voltage at half the input voltage. The examiner does not see any reason that precludes the combining of Nagai and Yao that would result in the combination being rendered inoperable.

Furthermore, the examiner admits that using the exact values of half the input voltage or three times the value of Va is not proper when the references are combined. However, the modified circuit achieves a different set of voltage values that are selected to properly render the device functional.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

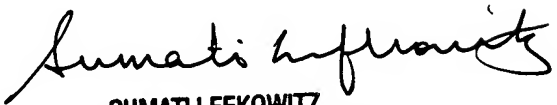
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donna V Lui
Examiner
Art Unit 2629



SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER